

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HTC CORPORATION and HTC AMERICA, INC.,<sup>1</sup>  
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,  
Patent Owner.

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Case IPR2015-01501  
Patent 7,777,753 B2

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Before JAMES B. ARPIN, MATTHEW R. CLEMENTS, and  
SUSAN L. C. MITCHELL, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

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<sup>1</sup> Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; and LG Electronics, Inc. were terminated from this proceeding. *See* Papers 28 and 42.

## I. INTRODUCTION

In its Petition requesting *inter partes* review, HTC Corporation and HTC America, Inc. (collectively, “Petitioner”) asserted the unpatentability of claims 1–4, 7–10, and 12 of U.S. Patent No. 7,777,753 B2 (Ex. 1001, “the ’753 patent”), owned by Parthenon Unified Memory Architecture LLC (“Patent Owner”). Paper 1 (“Pet.”), 1. The Petition identifies HTC Corporation; HTC America, Inc.; LG Electronics, Inc.; LG Electronics U.S.A., Inc.; LG Electronics MobileComm U.S.A., Inc.; Samsung Electronics Co., Ltd.; and Samsung Electronics America, Inc. as real parties-in-interest. *Id.* at 2. We have jurisdiction under 35 U.S.C. § 6, and this Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during the review. For the reasons discussed below, we determine that Petitioner has met its burden to prove, by a preponderance of the evidence, that claims 1–4 (“the challenged claims”) of the ’753 patent are unpatentable on the grounds upon which we instituted *inter partes* review.

### A. *Procedural History*

On June 24, 2015, Petitioner filed a Petition to institute an *inter partes* review of claims 1–4, 7–10, and 12 of the ’753 patent. Pet. 1. Petitioner asserted grounds for unpatentability based on the following references and declarations:

Exhibit	References and Declarations
1002	File History of Patent No. US 7,777,753 B2
1003	Patent No. US 5,546,547 (“Bowes”)

Exhibit	References and Declarations
1004	International Organization for Standardization, “ISO/IEC 11172-2: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video,” (1st ed. Aug. 1, 1993) (“MPEG”)
1007	Patent No. US 5,774,676 (“Stearns”)
1008	Declaration of Santhana Chari, Ph.D.
1019	T. Shanley <i>et al.</i> , “PCI System Architecture,” Addison-Wesley Publ’g Co. (3rd ed. Feb. 1995) (“Shanley”)
1020	H. Stone, “Microcomputer Interfacing,” Addison-Wesley Publishing Co. (1982)
1030	Declaration of Harold S. Stone, Ph.D. (the “Stone Decl.”)

Pet. vi–vii. Patent Owner filed a Preliminary Response (Paper 7). On January 6, 2016, we issued an Institution Decision (Paper 12, “Inst. Dec.”), instituting *inter partes* review on the following grounds:

References	Basis	Claim(s) challenged
Bowes and MPEG	35 U.S.C. § 103(a)	1 and 2
Bowes, MPEG, and Stearns	35 U.S.C. § 103(a)	3
Bowes, MPEG, and Shanley	35 U.S.C. § 103(a)	4

Inst. Dec. 8; *see* Pet. 5–6.

After institution, Petitioner filed a Request for Rehearing (Paper 14), which we denied (Paper 17), seeking reconsideration of our denial of institution of review with respect to claims 7–10 and 12. Patent Owner then filed a Patent Owner Response to the Petition (Paper 21, “PO Resp.”), and Petitioner replied (Paper 32, “Reply”). A hearing for the instant proceeding and related Cases IPR2015-01500 and IPR2015-01502 was held on September 19, 2016. A transcript (Paper 52, “Tr.”) of that hearing is included in the record.

*B. Related Proceedings*

The '753 patent is involved in several cases pending in the U.S. District Court for the Eastern District of Texas. Pet. 2–3; Paper 5, 2–3. Petitioner also has filed other petitions seeking *inter partes* review of related patents in related Cases IPR2015-01500 and IPR2015-01502. Pet. 3. Further, an unrelated petitioner, Apple Inc., has filed a petition challenging claims of the '753 patent. *See* IPR2016-01114, Paper 7, 2–3 & 42 (instituting *inter partes* review of claims 1–4, 7–10, and 12).

II. THE '753 PATENT (EX. 1001)

*A. Subject Matter*

The '753 patent relates generally “to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.” Ex. 1001, col. 1, ll. 36–41. As of the effective filing date of the '753 patent,<sup>2</sup> a typical decoder included a dedicated memory, which represented a significant percentage of the cost of the decoder and which went unused most of the time. *Id.* at col. 2, ll. 21–63, col. 4, ll. 43–60, Figs. 1a–1c.

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<sup>2</sup> The '753 patent claims the benefit of a string of earlier-filed U.S. patent applications, the earliest of which was filed on August 26, 1996. Ex. 1001 at [63]. Petitioner does not challenge the entitlement of the '753 patent to this earliest filing date and argues that the '753 patent expired in August of 2016, presumably based on this earliest filing date. Pet. 10–11. Patent Owner implicitly claims entitlement of the '753 patent to the benefit of this earliest filing date and expressly states that the '753 patent expired on August 26, 2016. Paper 8, 1.

To address these and other concerns, the '753 patent discloses an electronic system in which a first device and a video and/or audio decompression and/or compression device are coupled to a shared memory through a bus that may have bandwidth sufficient for the video and/or audio decompression and/or compression device to operate in real time. *Id.* at col. 4, l. 64–col. 5, l. 7. Figure 2 of the '753 patent is reproduced below.

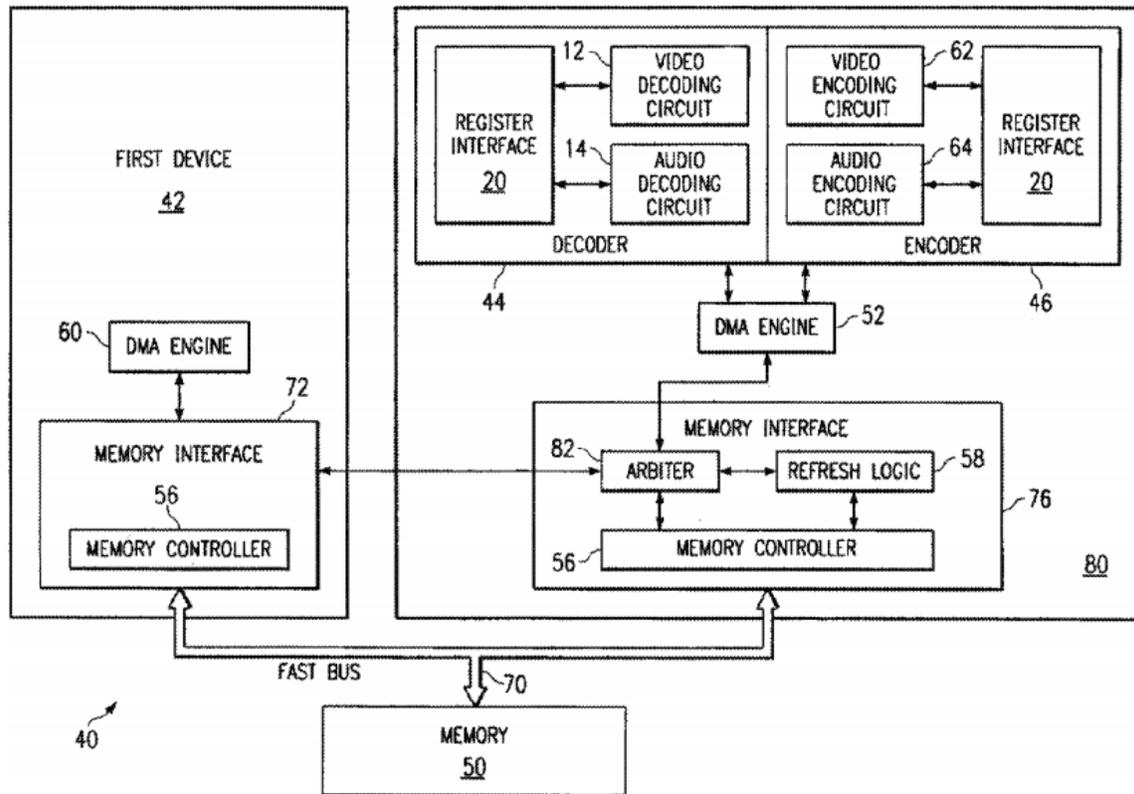


Fig. 2

Figure 2 is a block diagram of an electronic system that contains a device with a memory interface and an encoder and decoder. *Id.* at col. 6, ll. 3–5. “First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50 . . . .” *Id.* at col. 6, ll. 29–32. Both first device 42 and decoder/encoder 80 have access to memory 50 through memory interfaces 72 and 76, respectively,

coupled to fast bus 70. *Id.* at col. 6, ll. 27–29, col. 7, ll. 26–28, 48–51. Fast bus 70 may have at least the bandwidth required for decoder/encoder 80 to operate in real time and, preferably, has a bandwidth of at least approximately twice the bandwidth required for decoder/encoder 80 to operate in real time. *Id.* at col. 7, ll. 48–51, col. 8, ll. 28–33.

During operation, decoder/encoder 80, first device 42, and refresh logic 58, if it is present, request access to memory 50 through arbiter 82. *Id.* at col. 12, ll. 53–56. Arbiter 82 determines which of the devices may access memory 50. *Id.* at col. 12, ll. 57–58. Decoder/encoder 80 may get access to memory 50 in the first time interval, and first device 42 may get access to memory 50 in the second time interval. *Id.* at col. 12, ll. 58–61. Direct Memory Access (DMA) engine 52 of decoder/encoder 80 determines the priority of decoder/encoder 80 for access to memory 50 and the burst length when decoder/encoder 80 has access to memory 50. *Id.* at col. 12, ll. 61–67. DMA engine 60 of first device 42 determines its priority for access to memory 50 and the burst length when first device 42 has access to memory 50. *Id.* at col. 12, ll. 65–67.

When decoder/encoder 80 or one of the other devices generates a request to access memory 50, the request is transferred to arbiter 82, and access to memory 50 is determined based on the state of arbiter 82 and on a priority scheme. *Id.* at col. 13, ll. 1–30. In particular,

[t]he state of the arbiter 82 is determined. The arbiter typically has three states. *The first state is idle* when there is no device accessing the memory and there are no requests to access the memory. *The second state is busy* when there is a device accessing the memory and there is no other request to access the memory. *The third state is queue* when there is a device

accessing the memory and there is another request to access the memory.

*Id.* at col. 13, ll. 3–10 (emphases added). The priority scheme can be any scheme that ensures decoder/encoder 80 gets access to memory 50 often enough to operate properly, but does not starve entirely other devices sharing memory 50. *Id.* at col. 13, ll. 31–37; *see id.* at col. 8, ll. 9–13 (describing a “starvation period”).

*B. Illustrative Claim*

Of the challenged claims, claim 1 is independent. Ex. 1001, col. 15, ll. 32–59. Claims 2–4 depend directly from claim 1. *Id.* at col. 15, l. 60–col. 16, l. 9. Claim 1 is illustrative and is reproduced below:

1. An electronic system comprising:
  - a bus;
  - a main memory coupled to the bus having stored therein data corresponding to video images;
  - a video circuit coupled to the bus, the video circuit configured to receive data from the main memory corresponding to a current video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device, the current video image to be displayed adapted to be stored in the main memory;
  - a processor coupled to the main memory, the processor for storing non-image data in the main memory and retrieving non-image data from the main memory; and
  - an arbiter circuit coupled to the processor and to the video circuit, the arbiter circuit configured to receive requests for access to the main memory from the video circuit and the processor and to control access to the main memory by:
    - providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state;

queuing a request for access to the main memory when the arbiter circuit is in a busy state; and

queuing a request for access to the main memory in an order based on a priority of the request and a priority of each of one or more other requests for access to the main memory that are currently queued when the arbiter circuit is in a queue state.

Ex. 1001, col. 15, ll. 32–59.

### III. CLAIM CONSTRUCTION

Petitioner argues that the '753 patent expired in August of 2016. Pet. 10–11. Patent Owner states that the '753 patent expired on August 26, 2016. Paper 8, 1. Thus, the parties agree that the '753 patent has expired.

As a result, we construe the claims in accordance with the principles followed in district court. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b); *see Toyota Motor Corp. v. Cellport Sys., Inc.*, Case IPR2015-00633, slip op. at 8–10 (PTAB Aug. 14, 2015) (Paper 11); *cf. In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“While claims are generally given their broadest possible scope during prosecution, the Board’s review of the claims of an expired patent is similar to that of a district court’s review.”) (internal citation omitted). Although Petitioner proposed a construction of the term “decoder” under the broadest reasonable construction standard, Petitioner argues that its proposed construction will remain the same even if we apply the district court claim construction, consistent with the principles set forth in *Phillips*. Pet. 11 (stating that “this change in standards would not affect any of the proposed grounds in this Petition, especially in view of Patent Owner’s interpretations of the claims under the *Phillips* standard.”).

In our Decision on Institution, we construed the term “decoder” to mean “hardware and/or software that translates data streams into video or audio information.” Inst. Dec. 9–10. Neither party disputes our determination. *See* Tr. 15:24–16:17, 51:19–52:20. Nevertheless, the term “decoder” is not recited in challenged claims 1–4.

Neither Petitioner nor Patent Owner offers other constructions of any claim term *in the challenged claims*. *See* Pet. 8–11. Only terms which are in controversy in this proceeding need to be construed, and then only to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that “claim terms need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). For purposes of this Final Written Decision, no claim terms require express construction.

#### IV. ANALYSIS

Petitioner asserts that claims 1–4 of the ’753 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes and MPEG, alone or in combination with Shanley or Stearns. *See supra* Section I.A. Petitioner also relies upon the declaration of its declarant, Dr. Stone. *See* Ex. 1030 ¶¶ 153–174 (claims 1 and 2), 175–179 (claim 3), 180–181 (claim 4).

##### A. *Obviousness Over Bowes and MPEG*

###### 1. *Overview*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are “such that the subject matter[,] as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;<sup>3</sup> and (4) objective evidence of nonobviousness, i.e., secondary considerations.<sup>4</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).<sup>5</sup> For the reasons set forth below, we determine that Petitioner has shown by a preponderance of the evidence that claims 1 and 2 of the ’753 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes and MPEG.

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<sup>3</sup> Petitioner proposes an assessment for a person of ordinary skill in the art. Pet. 11 (citing Ex. 1030 ¶¶ 78–81); *see* Ex. 2009 ¶ 24. Patent Owner’s declarant, Dr. Thornton, proposes an alternative assessment for a person of ordinary skill in the art. Ex. 2009 ¶ 25. Nevertheless, Dr. Thornton testifies that “my analysis and conclusions would remain unchanged” regardless of which assessment is applied. *Id.* ¶ 26; *see* Tr. 40:8–42:11, 76:20–77:9. To the extent necessary and for purposes of this Final Written Decision, we adopt Petitioner’s assessment, which each party’s declarant meets or exceeds. *See* Ex. 1030 ¶¶ 2–6; Ex. 2009 ¶¶ 5–11.

<sup>4</sup> Patent Owner does not contend in the Patent Owner Response that such secondary considerations are present. *See* Paper 13, 6 (“Patent Owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.”).

<sup>5</sup> There is no requirement to enumerate each *Graham* factor and to include findings specifically in terms of the factors as long as “the required factual determinations were actually made and it is clear that they were considered while applying the proper legal standard of obviousness.” *Specialty Composites v. Cabot Corp.*, 845 F.2d 981, 990 (Fed. Cir. 1988).

*a. Bowes (Ex. 1003)*

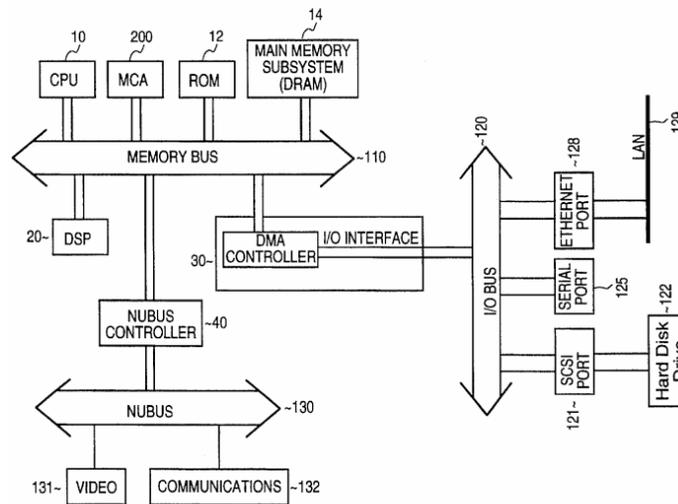
Bowes describes a memory bus arbiter for a computer system having a DSP co-processor. Ex. 1003, Title. According to Bowes,

[i]n prior art computer systems, because of the high bandwidth required for real-time processing by a DSP, it has not been possible for the DSP to run off of the computer system's [dynamic random access memory (DRAM)] in the way the [central processor unit (CPU)] 10 utilizes it without adversely affecting the rest of the computer system. Thus, there has been provided a large block of [static random access memory (SRAM)] 24 for use by the DSP 20. . . .

A significant disadvantage to the prior art computer architecture of FIG. 1 is the requirement of a substantial block of static random access memory 24. SRAMs are significantly more expensive than DRAM which greatly increases the cost of computer systems which incorporate SRAM.

*Id.* at col. 2, ll. 36–48. Thus, it is an object of Bowes “to provide a mechanism and method for arbitrating the memory bus bandwidth to efficiently allow the use of a digital signal processor and a CPU over a common memory bus *sharing* the system's dynamic random access memory subsystem without requiring an expensive block static random access memory.” *Id.* at col. 2, ll. 57–63 (emphasis added).

Figure 2 of Bowes is reproduced below.



**Figure 2**

Figure 2 illustrates a block diagram of a computer architecture incorporating the arbitration scheme described in Bowes. *Id.* at col. 3, ll. 62–64. “The scheme is implemented such that the DSP is provided with sufficient bandwidth to perform real-time digital signal processing using the system’s [DRAM] and not requiring the incorporation of an expensive block of [SRAM].” *Id.* at col. 4, ll. 55–60. As shown in Figure 2, the system includes CPU 10, memory controller and arbiter (MCA) 200, main memory subsystem 14, and DSP 20. *Id.* at Fig. 2. “Unlike prior art computer systems, the [system of Bowes] provides for the DSP 20 to reside on the system’s memory bus and operate from the computer systems’ main memory subsystem 14.” *Id.* at col. 6, ll. 22–26. “[T]his greatly reduces system cost by eliminating the need for an expensive block of SRAM.” *Id.* at col. 6, ll. 26–29. In a preferred embodiment, MCA 200 “is an application[] specific integrated circuit (ASIC) for arbitrating memory bus 110 between the various bus masters subject to the constraints each imposes

to provide optimal bandwidth for each, particularly the DSP which is responsible for a significant amount of real-time signal processing.” *Id.* at col. 6, ll. 46–52.

*b. MPEG (Ex. 1004)*

MPEG describes the coded representation of video for digital storage media and specifies the decoding process for the MPEG-2 standard.

Ex. 1004, 1. The MPEG standard was known and accessible at least as of August of 1993. Ex. 1008 ¶ 8.

*2. Analysis*

We are persuaded by Petitioner’s arguments and cited evidence that the combination of the teachings of Bowes and MPEG teaches or suggests all of the recited limitations of challenged claims 1 and 2. Pet. 38–47; *see* Inst. Dec. 24–29. In particular, Bowes discloses supporting video applications (Ex. 1003, col. 1, ll. 24–41), and specifically discloses video controllers 131 coupled to memory bus 110 (*id.* at col. 6, ll. 6–18). Pet. 39. Moreover, DSP 20 performs “image processing.” *Id.* (citing Ex. 1003, col. 6, ll. 33–38). Thus, Petitioner argues that Bowes discloses that both CPU 10 (i.e., the “processor” of claim 1) and DSP 20 (i.e., the “video circuit” of claim 1) are attached to memory bus 110, from which they access main memory subsystem 14. Pet. 39. In addition, Petitioner argues that Bowes discloses an arbiter (i.e., MCA 200) and each of the arbiter functions of “providing access” in an idle state (Ex. 1003, col. 7, l. 64–col. 8, l. 10, col. 8, ll. 28–35), “queuing a request for access” in a busy state (*id.* at col. 8, ll. 50–55, 63–65), and “queuing a request for access . . . in an order based on a priority “ in a queue state (*id.* at col. 8, ll. 50–55, col. 9, ll. 2–6, 11–14). Pet. 44–46 (citing Ex. 1030 ¶¶ 168–170). We agree.

Petitioner further contends that a person of ordinary skill in the art would have found it obvious to combine the teachings of *Bowes* and MPEG to achieve the systems, methods, and circuits limitations recited in the challenged claims.

*Bowes* discloses that DSP 20 performs “image processing,” *id.*, 6:33-38, which *MPEG Standard* (see generally Ex. 1030 at ¶ 83) discloses includes video image decoding. Ex. 1004 at 7-8 (“0.4 Decoding”), 42 (“2.4.4. The video decoding process”). In MPEG video decoding, *MPEG Standard* teaches, some currently decoded video images are stored for decoding subsequent video images. See, e.g., Ex. 1004 at 8 (§ 0.4) (“After all the macroblocks in the picture have been processed, the picture has been reconstructed. If it is an I-picture or a P-picture it is a reference picture for subsequent pictures and is stored, replacing the oldest stored reference picture.”).

*Bowes* contemplates supporting video applications, Ex. 1003 at 1:24-41, and discloses video controllers 131 coupled to memory bus 110, *id.*, 6:6-18. One of ordinary skill in the art would have been motivated to modify *Bowes*’ DSP 20 in view of *MPEG Standard* to perform MPEG video decoding. At the time of the alleged invention of the ’753 patent, the MPEG-1 and MPEG-2 standards were “currently in use.” Ex. 1001, 1:53-58. Indeed, the ’753 patent admits that “[t]he MPEG standards [were] currently well accepted standards.” Ex. 1001, 2:6-9. Thus, modifying *Bowes*’ DSP 20 to perform MPEG video decoding per *MPEG Standard* would constitute a combination of familiar elements according to known methods to yield predictable results. See *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); see also Ex. 1030, Stone Decl. ¶¶ 157-61. Indeed, the MPEG Standard “was developed in response to the growing need for a common format representing compressed video on various digital storage media,” which would have motivated on skilled in the art to modify *Gulick*’s multimedia engine 112 to perform MPEG video decoding. Ex. 1004 at 4 (§ 0.1)[; see Pet. 29]. In fact, it was well known in the art at the time of the alleged invention to employ a DSP for MPEG video processing. See Ex.

1017, 5:15-21; Ex. 1007, 1:62-67, Fig. 5. One of ordinary skill in the art would have understood that *Bowes's* DSP 20, as modified by *MPEG Standard*, would be configured to receive data from main memory subsystem 14 corresponding to a current video image to be MPEG-video decoded and to output video data corresponding to the current video image to be displayed via video controllers 131, the current video image to be displayed adapted to be stored in main memory subsystem 14. Ex. 1030, Stone Decl. ¶¶ 162-63.

Pet. 40–42. In contrast, Dr. Thornton testifies that

the fact that *Bowes* not once mentioned the implementation of the MPEG standard or for that matter, any implementation involving video decoding, further indicates that a [person of ordinary skill in the art (POSA)] would not have been motivated to combine *Bowes* with the MPEG Standard as the Petitioner suggests.

Ex. 2009 ¶ 86. We find Dr. Thornton's testimony unpersuasive. *See* Reply 21–22. The challenged claims also do not mention the MPEG Standard. The question is not whether *Bowes* expressly teaches use of the MPEG Standard, rather the question is whether a person of ordinary skill in the art would have combined the teachings of *Bowes* and the MPEG Standard in the manner recited in the challenged claims. *KSR*, 550 U.S. at 424 (“The proper question to have asked was whether a pedal designer of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to upgrading *Asano* with a sensor.”). We are persuaded that a person of ordinary skill in the art would have had reason to incorporate the known MPEG Standard into *Bowes's* system and that doing so would have yielded predictable results, in order to satisfy the “growing need for a common format representing compressed video on various digital storage media.” Pet. 41–42; Reply 17; *see* Ex. 1032 ¶¶ 84–88.

Patent Owner contends that Petitioner fails to demonstrate by a preponderance of the evidence that claims 1 and 2 of the '753 patent are obvious over the applied art for four reasons. PO Resp. 3–42. Specifically, Patent Owner contends that (a) the combination of the teachings of Bowes and MPEG does not teach “providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state” (*id.* at 3–5); (b) the combination of the teachings of Bowes and MPEG does not teach “wherein the video circuit is further configured to receive data from the main memory corresponding to at least one previously decoded video image” (*id.* at 5–26); (c) the combination of the teachings of Bowes and MPEG does not teach “an arbiter that controls access to the main memory” (*id.* at 26–32); and (d) a person of ordinary skill in the art would not have had reason to combine the teachings of Bowes and MPEG (*id.* at 32–41). We address each contention in turn.

- a. *“providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state” (Claim 1)*

Patent Owner contends that the combined teachings of Bowes and MPEG do not teach or suggest this limitation of challenged claim 1 because “the arbiter of Bowes does not have an ‘idle state.’” *Id.* at 3 (citing Ex. 2009 ¶ 33). We disagree.

As noted above, claim 1 recites that the arbiter “provid[es] access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state.” Ex. 1001, col. 15, ll. 46–53. In the “idle state,” “there is no device accessing the memory and there are no requests to access the memory.” *Id.* at col. 13, ll. 4–6. Petitioner argues that Bowes teaches a “default” state during which no other devices are requesting access to the memory bus, MCA 200 is idle, and memory bus 110 is assigned by default to, i.e., “remains parked on,” CPU 10, until some other device requests memory bus 110. Pet. 44 (quoting Ex. 1003, col. 8, ll. 28–35). Further, Petitioner argues that, when MCA 200 is in this default state, MCA 200 may provide access to CPU 10 *by default* or to some other device, such as DSP 20, upon receipt of a request. *Id.* As discussed below, we are persuaded that access to the memory bus is tantamount to access to the main memory.

Patent Owner contends, however, that, because Bowes’s system assigns access to CPU 10 *by default*; “in Bowes, even if there are no requests to access the memory, the CPU is given access to the memory.” PO Resp. 4 (citing Ex. 2009 ¶ 34). According to Patent Owner, because CPU 10 is given access by default, it is not the case in Bowes that *no* device is accessing the memory. *Id.* Nevertheless, Patent Owner conflates the concepts of being given access, e.g., the memory bus being *assigned* to a device, and accessing. Reply 3; *see* Tr. 45:5–46:10, 82:17–84:23 (discussing the difference between *assignment* and *accessing*). Although Bowes’s system *assigns* access to CPU 10 in the default state, this does not mean that CPU 10 *accesses* the memory bus. *See* Ex. 1032 ¶ 91. Thus, Bowes’s default state does not preclude the situation in which CPU 10 has

been assigned access to the memory bus, but currently is not accessing the memory bus. Reply 2; *see* Ex. 1001, col. 8, ll. 29–30 (“the CPU 10 does not issue bus request signals”), 32–34 (“The CPU is also provided with one time slot in the priority scheme . . . in which it is granted the memory bus.”).

For these reasons, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Bowes and MPEG teach this limitation of challenged claim 1.

*b. “the video circuit is further configured to receive data from the main memory corresponding to at least one previously decoded video image” (Claim 2)*

Patent Owner contends that the combined teachings of Bowes and MPEG do not teach or suggest this limitation of challenged claim 2 for three reasons. First, Bowes does not teach a video circuit that is linked to a main memory, rather than a dedicated memory. PO Resp. 5–8, 11–19. Second, Bowes does not teach that its DSP receives a previously decoded video image from the main memory. *Id.* at 8–11, 19–24. Third, Bowes does not teach that the DSP reads data from and writes data to a main memory. *Id.* at 24–26. Again, we disagree with each of Patent Owner’s reasons.

*i. Whether Bowes’s DSP Teaches a “Video Circuit”*

Patent Owner asserts that Bowes’s DSP does not teach a “video circuit,” as recited in the challenged claims. *Id.* at 11–19. In particular, Patent Owner contends that Bowes only mentions the word “video” four times and only once in relation to its system. *Id.* at 11. Bowes only uses the word “video” in relation to the NuBus peripheral bus *video* controller and not in relation to DSP 20. *Id.* Consequently, Patent Owner contends that “Bowes does not state that the DSP is suitable for video compression and

decompression applications such as the MPEG Standard” (*id.* at 11 (citing Ex. 2009 ¶ 47)), and that “a [person of ordinary skill in the art] would recognize that audio processing, speech processing and modem emulation are clearly distinct from video compression and decompression. The same is true with respect to ‘image processing.’” (*id.* at 11–12 (citing Ex. 2009 ¶ 47)). *See* Tr. 62:11–65:4.

Although Bowes explicitly teaches the use of DSP 20 for “image processing” (Ex. 1003, col. 6, l. 35), Bowes does not teach explicitly the use of DSP 20 for video compression and decompression. The grounds of unpatentability, however, are based upon a *modification* of the teachings of Bowes’s DSP 20 to perform video decoding according to the MPEG Standard. Pet. 41 (“Bowes contemplates supporting video applications, Ex. 1003 at 1:24-41, and discloses video controllers 131 coupled to memory bus 110, *id.*, 6:6-18. One of ordinary skill in the art would have been motivated to modify Bowes’ DSP 20 in view of MPEG Standard to perform MPEG video decoding.”); *see* Ex. 1030 ¶¶ 162–63. Dr. Stone testifies that “Bowes discloses that DSP 20 performs ‘image processing,’ Ex. 1003 at 6:33-38, which MPEG Standard discloses includes video image decoding, Ex. 1004 at 7-8 (§ 0.4 Decoding), 42 (§ 2.4.4. The video decoding process).” Ex. 1030 ¶ 158. Bowes further teaches that DSP 20 “may be an off-the-shelf DSP.” Ex. 1003, col. 2, ll. 21–22.

As noted above, neither party has proposed a construction for “video circuit.” *See supra* Section III. Moreover, neither the challenged claims nor the Specification of the ’753 patent requires that the “video circuit” must be suitable for video decompression, and “neither Patent Owner nor its expert dispute that the prior art included ‘off the shelf’ DSPs capable of video

compression and decompression pursuant to the *MPEG Standard* or that a skilled artisan could have implemented the Bowes/MPEG combination using such prior art DSPs.” Reply 4 (citing Ex. 1032 ¶¶ 8–10); *see also* Ex. 1032 ¶ 10 (“[A] person of skill would understand Bowes to be pointing out that any available DSP could potentially be used in the system of Bowes”)(citing Exs. 1006, 1035, 1036, 2008); Ex. 1023, col. 6, ll. 20–22 (“digital system chip 112 also preferably includes *a general purpose DSP engine 206 which is programmable to perform various functions such as MPEG decoding.*” (emphasis added)). Thus, even assuming that Bowes’s “image processing” does not teach video decompression expressly, we, nevertheless, are persuaded that “off the shelf” DSPs existed that were capable of decompressing MPEG video, and that it was within the level of ordinary skill in the art to use, in the system of Bowes, such a DSP as DSP 20 to operate in accordance with the well-known MPEG standard. *See* Ex. 1008 ¶ 8 (“As a published standard, those in the field of image/video coding . . . would have known about, sought out, and had access to the *MPEG Standard*, at least as of August 1993.”); *KSR*, 550 U.S. at 421 (“When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.”).

Patent Owner also contends that DSP 20 is not suitable for video decompression because it is a floating-point DSP. PO Resp. 12–16. Initially, we note that Bowes does not mention “fixed” or “floating” point DSPs. *See* Tr. 91:15–20; *but see id.* at 66:20–25. This contention is not persuasive because it is based on an exemplary implementation provided in Bowes, namely the use of the AT&T DSP3210. Reply 5–6; *see* Ex. 1001,

col. 6, ll. 28–30 (“In the *preferred embodiment implementation*, the DSP 20 is an AT&T DSP3210 which provides an internal 8K SRAM cache.” (emphasis added)). The teachings of Bowes, however, are not limited to the use of the AT&T DSP3210 as DSP 20. Moreover, Patent Owner’s contention that the AT&T DSP3210 is too slow to decode MPEG images is not adequately supported by evidence. Reply 6–7 (quoting Ex. 1037, 66:5–12, 67:8–14, 69:2–8 (emphasis added)), 7–8 (alleging that Dr. Thornton’s testimony contains errors); *see* Tr. 91:21–92:4 (citing Ex. 1032 ¶¶ 12–17); *cf.* PO Resp. 16.

Finally, Patent Owner contends that its assertion that “the DSP of Bowes is not suitable for video compression and decompression is further evident from the way that DSP is used in the industry.” PO Resp. 17 (citing Ex. 2009 ¶ 55). Apple Inc., the assignee of Bowes, did not use the AT&T DSP3210 chip for processing video in its Quadra product. *Id.* at 17–18. There is no evidence, however, why Apple Inc. made the choices it made when designing the Quadra and when it made those choices. Patent Owner’s reasoning is based upon an assumption that Apple Inc. would have used the AT&T DSP3210 for video processing if the AT&T DSP3210 had been capable of video processing, but we find no support for that assumption in this record. *See* Reply 8. We do not find this contention persuasive.

Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Bowes’s DSP teaches a “video circuit.”

*ii. Whether Bowes and MPEG Teach Using a Dedicated Memory, Rather Than a Shared Memory*

Patent Owner also contends that, even if a person of ordinary skill in the art had combined the teachings of Bowes and MPEG, the combination

would have used a dedicated memory for the video circuit. PO Resp. 19–24. Patent Owner points to the local dedicated cache of the AT&T DSP3210, an exemplary embodiment of DSP 20, and contends that a person of ordinary skill in the art “would have used a larger dedicated memory with sufficient space to store an image frame and that the DSP would retrieve the previously decoded image from this dedicated memory” in order to “(a) eliminate the need for the DSP to access the memory bus during the decoding process; (b) allow other devices to access the memory bus during video decoding; (c) provide faster access by the DSP to a previously decoded image; and (d) free up space in the main memory.” *Id.* at 20 (citing Ex. 2009 ¶ 60).

We credit the testimony of Dr. Stone, however, that a person of ordinary skill in the art would have had reason *not* to use a cache to hold image data because such a system would “not guarantee that you could retrieve it” (Ex. 2006, 159:22–23) and that, even if one did use the cache to hold the image data, the image data “will also be backed up to main memory” (*id.* at 163:22–23). Reply 10; *see also* Ex. 1032 ¶ 32 (“[I]f you stored the data in the DSP cache, you could not reliably retrieve it from the cache because it could have been evicted from the cache when you attempted to retrieve it at a later time.”). Moreover, Patent Owner’s contention that a person of ordinary skill in the art would have had reason to modify the teachings of Bowes’s DSP 20 to include a dedicated image memory is contrary to a stated purpose of Bowes, which is to eliminate a block of dedicated SRAM. *See* PO Resp. 20–21.

The present invention concerns a computer architecture in which a digital signal processor (DSP) operates as a true co-processor

in the computer system. That is, an arbitration technique and mechanism are implemented which allows a DSP to reside on the system's CPU or memory bus and share the memory bus resources with the other potential bus masters on the memory bus. *The scheme is implemented such that the DSP is provided with sufficient bandwidth to perform real-time digital signal processing using the system's dynamic random access memory (DRAM) and not requiring the incorporation of an expensive block of static random access memory (SRAM).* DRAM is far less expensive than SRAM and the elimination of a block of SRAM greatly reduces the cost of computer systems.

Ex. 1003, col. 4, ll. 49–62 (emphasis added); *see* Reply 11.

Patent Owner also contends that Dr. Stone confirmed that a person of ordinary skill in the art would have used dedicated memory, rather than a shared memory. PO Resp. 20 (citing Ex. 2006, 134:23–142:22). Dr. Stone's testimony, however, merely explains when the use of shared memory is advantageous—e.g., “if I could reduce the total amount of memory or the total volume or something like that” (Ex. 2006, 140:24–141:1)—and when it may not be advantageous—e.g., if it “causes you to use more memory than if you had dedicated memory” (*id.* at 142:8–9). This testimony does not undermine Petitioner's arguments because Patent Owner provides no evidence that, in the combination of the teachings of Bowes and MPEG proposed by Petitioner, the shared memory architecture always would require the use of more memory than a dedicated memory architecture. Further, Patent Owner contends that, “[a]bsent a local dedicated memory available to the DSP of Bowes, this goal would be unattainable as a DSP that operates faster than the clock rate of the rest of the modules of the computer system would nevertheless have to wait on the slower system accesses available to the main memory.” PO Resp. 24 (citing

Ex. 2009 ¶ 66). All goals of the invention, however, need not be achieved by each embodiment. *ScriptoPro LLC v. Innovation Associates, Inc.*, 833 F.3d 1336, 1341 (Fed. Cir. 2016) (“But a specification’s focus on one particular embodiment or purpose cannot limit the described invention where that specification expressly contemplates other embodiments or purposes.”). Reduced volume of memory is not the only factor that can make shared memory advantageous; Bowes itself teaches another advantage, namely, “DRAM is far less expensive than SRAM and the elimination of a block of SRAM greatly reduces the cost of computer systems.” Ex. 1003, col. 4, ll. 61–62; see *In re Nuvasive, Inc.*, Dkt No. 2015-1670, 2016 WL 7118526, at \*4 (Fed. Cir. Dec. 7, 2016) (“Our recent decisions demonstrate that the PTAB knows how to meet this burden. For example, in *Nike, Inc. v. Adidas AG*, we affirmed the PTAB’s finding of a motivation to combine where it determined that a PHOSITA “interested in Nishida’s preference to *minimize waste in the production process* would have logically consulted the well-known practice of flat-knitting, which eliminates the cutting process altogether.” (emphasis in original, internal citations omitted)).

Patent Owner also contends that a person of ordinary skill in the art would not use the bandwidth on the bus and storage space in the main memory to store the previously decoded images (i.e., the “T” and “P” image frames) that are generated during the decoding process, knowing that those previously decoded images have to be retransmitted back to the decoder to decode upcoming “P” and “B” image frames.

PO Resp. 22. This contention is unavailing, however, because it is based upon “an implementation using DSP3210” (*id.* at 22–23) to which Bowes is not limited, and because Bowes explicitly describes DSP 20 reading from and writing to DRAM—i.e., the recited “main memory:”

[T]he DSP will utilize the memory bus 110 [] to read a large block memory from the DRAM 14 into its internal SRAM. Another mode of operation concerns the handling of data that has already been processed by the DSP. In many cases it will be necessary to push that data back out to the DRAM so that some other parts of the computer system can utilize it. Thus, the capability of bursting data out is a second mode of operation which may be referred to further herein as a “block write”.

Ex. 1003, col. 7, ll. 3–12. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Bowes teaches use of a shared memory, rather than a dedicated memory. Reply 12–13.

*iii. Whether Bowes’s DSP Writes Data to a Main Memory and Reads the Data it Stores From the Main Memory*

Patent Owner also contends that “[t]o the extent Bowes discloses the DSP (20) storing data in the main memory (14), that data is stored for use by *other parts* of the system and Bowes does not disclose the DSP (20) itself accessing the data it stored in the main memory (14).” PO Resp. 25 (citing Ex. 2009 ¶ 67). Specifically, Bowes allegedly does not teach that its DSP reads the data that it stores in main memory. *Id.* at 24–26. According to Patent Owner, Bowes describes only two types of retrieval from the main memory: (1) large block memory retrieval and (2) “handling of data that has already been processed by the DSP.” *Id.* at 25 (quoting Ex. 1003, col. 7, ll. 2–12). Consequently, Patent Owner concludes that a person of ordinary skill in the art “would not have stored a previously decoded image in the main memory for subsequent access by the DSP.” *Id.*

In particular, Patent Owner contends that Bowes teaches a “block write” operation that “[i]n *many* cases . . . push[es] data back out to the DRAM,” but that data is stored for use only by “some other part of the computer system” to utilize. *Id.* at 25–26 (quoting Ex. 1003, col. 7,

ll. 2–12 (emphasis added)). As Petitioner correctly points out, however, the cited sentence in *Bowes* describes “many”—*but not all*—cases. Reply 13 (citing Ex. 1003, col. 7, ll. 6–12). Moreover, *Bowes* does not teach that data is pushed back out to DRAM *only* so that some other parts of the computer system can utilize it. *Id.* Therefore, Patent Owner’s conclusion is not supported by adequate evidence.<sup>6</sup>

In addition, Petitioner argues that

the *MPEG Standard* discloses that previously decoded images must be used decode at least some video images consistent with the MPEG standard, Ex. 1004 at 8, 42-48, 66-67; Fig. 4, and the Petition demonstrated that *Bowes* discloses a DSP 20 that will access main memory as needed to carry out real time signal processing, such as the processing required for video conferencing, Pet. at 40-42.

Reply 13–14. Thus, Petitioner argues that a person of ordinary skill in the art would have understood that the combined teachings of *Bowes* and MPEG teach a video circuit “that writes and reads image data to and from main memory in order to decompress video images pursuant to MPEG.” *Id.* at 14 (citing Pet. 41–42; Ex. 1030 ¶¶ 157–163; Ex. 1032 ¶¶ 43–44). We agree, and we credit Dr. Stone’s testimony on this point. Therefore, we are persuaded that Petitioner has demonstrated by a preponderance of the

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<sup>6</sup> Dr. Thornton’s testimony (Ex. 2009 ¶¶ 67–68) mirrors Patent Owner’s contentions almost verbatim (PO Resp. 25–26). Thus, Dr. Thornton’s testimony adds nothing to Patent Owner’s contentions. *See Infobionic, Inc. v. Braemer Manufacturing, LLC*, Case IPR2015-01704, slip op. at 13 (PTAB February 16, 2016) (Paper 11) (“Petitioner does not explain adequately why this is correct, and the cited expert testimony merely repeats the Petitioner’s conclusory argument, adding the phrase ‘[i]n my opinion’ (Ex. 1002 ¶ 39).”).

evidence that Bowes's DSP 20 writes data to a main memory and reads the data it stores from the main memory. *Id.* at 12–14.

*c. Whether Bowes's Arbiter Controls Access to Main Memory*

Patent Owner contends that the proposed combination does not disclose an arbiter that controls access to the main memory because Bowes's "MCA (200) (identified as the arbiter) arbitrates access to the memory bus (110), not the memory subsystem (14) identified by the Petition as the main/system memory." PO Resp. 27. Patent Owner contends that controlling access to memory is not the same as merely controlling access to a peripheral bus because (1) a device may be granted access to the bus without accessing main memory (*id.* at 28); (2) a bus arbiter grants access differently than a memory arbiter (*id.* at 28–29); and (3) a memory arbiter is more efficient than a bus arbiter (*id.* at 29–31).<sup>7</sup>

Patent Owner's contentions are unpersuasive because they are not commensurate with the scope of the claims, which do not recite, for example, (1) *guaranteeing* access to the memory; (2) "a memory arbiter;" or (3) controlling access to the memory or bus *most efficiently*. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability). As

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<sup>7</sup> Patent Owner also contends that the distinction between controlling access to the memory and controlling access to the bus is also evident from the claims of other patents from which the '753 patent claims priority. PO Resp. 31–32. Nevertheless, Patent Owner fails to explain a sufficient link between the drafting and/or prosecution of the claims of those related cases and the challenged claims of the '753 patent, for us to rely on the recitations of the related claims to limit the scope of the challenged claims. *See Ex. 1002*, 19 ("Reasons for Allowance").

Petitioner notes correctly, “claim 1 does not recite how access to the memory is controlled, so any technique of controlling access to the memory would satisfy that claim language.” Reply 14–15. As a result, we remain persuaded by Petitioner’s argument that MCA 200, by controlling access to the bus, also controls access to the main/system memory. *See* Pet. 43–44; *see also* Reply 14–17 (citing Ex. 1032 ¶¶ 46–51, 54–61, 63–69).

*d. Motivation to Combine*

Patent Owner contends that Petitioner has not articulated sufficiently a reason to combine the teachings of Bowes and MPEG. PO Resp. 32–41. Specifically, Patent Owner contends that:

A POSA would not have been motivated to combine Bowes with the MPEG Standard because: (1) Bowes does not disclose a video [circuit];<sup>8</sup> (2) at the time of filing of the ’753 Patent, a POSA would not deem using a shared memory between a [video circuit] and another device as being advantageous; (3) the Bowes’ arbitration scheme is incompatible with implementation of the MPEG Standard; and (4) the Bowes’ watchdog timer renders Bowes incompatible with the MPEG Standard.

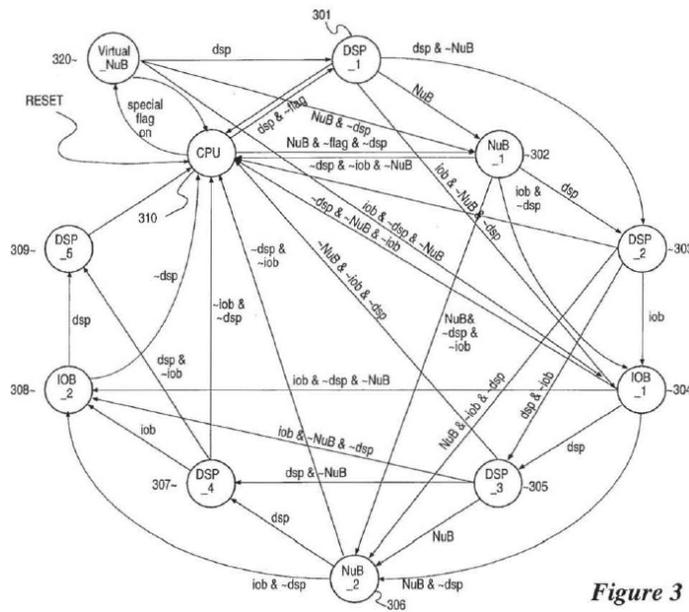
*Id.* at 32–33 (citing Ex. 2009 ¶ 75). We already have addressed contentions (1) and (2) above. With respect to contention (3), Patent Owner asserts that “the arbiter of Bowes adheres to a specific state diagram (shown in [Bowes’s] Figure 3) which allows for up to 10 time slots per arbitration cycle” (*id.* at 36 (citing Ex. 1003, col. 9, ll. 11–17)) and that “[t]he Bowes

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<sup>8</sup> Although Patent Owner refers to a “decoder,” the term “decoder” only appears in claims, for which we denied review. *See supra* Section III. We understand that Patent Owner intended to refer to the “video circuit” recited in challenged claims 1–4.

arbitration cycle would prevent the bus from being available to the DSP for a number of time slices (e.g., 5 of 10 time slices in the preferred embodiment of Figure 3) and would thus *likely* prevent the DSP from achieving the required data transfer rate due to bus unavailability” (*id.* at 38 (emphasis added; citing Ex. 2009 ¶ 81)). This contention is not persuasive.

Figure 3 of Bowes is reproduced below.



Ex. 1003, Fig. 3. Figure 3 depicts “a state diagram of the arbitration scheme for assigning bandwidth slots to the various components of the *preferred embodiment* computer architecture.” *Id.* at col. 4, ll. 1–3 (emphasis added). As an initial matter, Patent Owner asserts that the arbitration cycle “would *likely* prevent”—but not “would prevent”—the DSP from achieving the required data transfer rate,” an assertion which is insufficient to show that a person of ordinary skill in the art would have found Bowes’ arbitration scheme incompatible with implementation of the MPEG Standard. Reply 19; *see* PO Resp. 38. In addition, we do not agree that the state diagram shown in Figure 3 imposes a “strict and inflexible priority” (Ex. 2009 ¶ 81)

and requires stepping through all ten states. *See* Reply 19. Dr. Thornton acknowledges that Figure 3 depicts only a “preferred embodiment” of Bowes’s arbitration cycle. Ex. 2009 ¶ 81. Consequently, without more, Bowes’s teachings regarding its arbitration scheme are not limited to that embodiment. Moreover, referring to Figure 3, from state DSP\_1, for example, the state diagram proceeds to state NuB\_1 only if there is a request present from the NuBus controller (indicated in Figure 3 by the arrow labeled “NuB”). Ex. 1003, Fig. 3. If, however, there is no request present from the NuBus controller and there is a new request from the DSP (indicated by the arrow labeled “dsp & -NuB”), the state diagram proceeds to DSP\_2. *Id*; *see also id.* at col. 8, l. 65–col. 9, l. 2.

Our understanding of Figure 3, moreover, is consistent with Dr. Stone’s testimony. Reply 19–20; *see* Ex. 1032 ¶¶ 80–82. Because the arbitration scheme shown in Figure 3 could proceed directly from DSP\_1 to DSP\_2 to DSP\_3 to DSP\_4 to DSP\_5 without ever entering any of the NuB or IOB states, we are not persuaded by Patent Owner’s contention that the scheme shown in Figure 3 *necessarily* limits the DSP to only 5 of 10 time slots per arbitration cycle. *But see* Ex. 1032 ¶¶ 52–58. Even if Patent Owner were correct about Figure 3, it is merely a preferred embodiment, and the teachings of Bowes are not limited to the preferred embodiment. *See* Reply 17, 20.

With respect to contention (4), Patent Owner asserts that “Bowes discloses a watchdog timer (241) that counts the number of system clocks that the DSP has owned the memory bus in a given arbitration loop before terminating the DSP’s ownership of the memory bus” and that “this limitation on the DSP’s access to the main memory *could* render a

combination of Bowes with the MPEG Standard nonviable as it *could* prevent the DSP from decoding images in real-time.” PO Resp. 39–40 (emphases added) (citing Ex. 1003, col. 9, ll. 21–38). Specifically, Patent Owner contends that “the DSP of Bowes would be unable to access previously decoded images . . . from the main memory . . . within the required time limit set by the watchdog timer (241).” *Id.* at 40 (citing Ex. 2009 ¶ 85).

This contention also is not persuasive. Patent Owner asserts only that the limitation “could” render the combination nonviable and “could” prevent the DSP from decoding images in real-time, but does not argue that it “would” be nonviable. *See* Reply 20; Ex. 1032 ¶ 82. Patent Owner cites to paragraph 85 of Dr. Thornton’s declaration, but that paragraph merely repeats the language in the Petition. *Compare* PO Resp. 39–40 *with* Ex. 2009 ¶ 85; *see supra* pg. 26 n.6. Moreover, Bowes teaches watchdog timer 241 in the context of “*Alternative DSP Operation Modes.*” Ex. 1003, col. 9, l. 19 (emphasis added). Also, Petitioner counters that an entire image need not be read from main memory before the watchdog timer runs out because “the system could make multiple reads of data from the memory, each within the time period permitted by the timer.” Reply 21 (citing Ex. 1032 ¶ 82). We note the lack of definiteness in Dr. Thornton’s testimony, and we credit Dr. Stone’s testimony here. Based on our assessment of the testimony and the teachings of Bowes and of Petitioner’s arguments, we are not persuaded that a person of ordinary skill in the art would have understood Bowes’s teachings regarding watchdog timer 241 to mean that a DSP using Bowes’ arbitration scheme *would not* be capable of decoding video.

On this record, therefore, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

3. *Conclusion*

We are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1 and 2 of the '753 patent are unpatentable as obvious over the combination of the teachings of Bowes and MPEG

B. *Claim 3 — Obviousness over Bowes, MPEG, and Stearns*

Petitioner argues that claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Stearns. Pet. 47–49.

1. *Stearns (Ex. 1007)*

Stearns describes a computer architecture in which MPEG accelerator functionality is integrated with a graphics accelerator. Ex. 1007, col. 6, ll. 14–23, Fig. 4.

2. *Analysis*

Claim 3 depends directly from independent claim 1. As discussed above, we are persuaded that Petitioner has established by a preponderance of the evidence that independent claim 1 would have been obvious over the combination of Bowes and MPEG. *See supra* Section IV.A. Petitioner relies upon Stearns only for the additional limitations recited in dependent claim 3. Pet. 47–49. We are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Stearns teaches or suggests these additional limitations and that a person of ordinary skill in the art would have had reason to combine Stearns's teachings with those of Bowes and

MPEG. *Id.* Moreover, Patent Owner does not dispute that Stearns teaches or suggests the additional limitations of claim 3 or that a person of ordinary skill in the art would have had reason to combine Stearns’s teachings with those of Bowes and MPEG. PO Resp. 41; *see* Ex. 1030 ¶¶ 175–179 (arguing persuasively that Stearns shows the additional limitations of claim 3 and that a person of ordinary skill in the art would have had reason to modify the combined teachings of Bowes and MPEG in view of the teachings of Stearns to achieve the challenged claim); *see also* Paper 13, 6 (arguments not raised in the Patent Owner Response are deemed waived).

Instead, Patent Owner contends that Stearns does not teach or suggest the limitations of claim 1 allegedly missing from the combined teachings of Bowes and MPEG. PO Resp. 41. Patent Owner contends only that “independent claim 1 is also not obvious in view of the proposed combination of Bowes, the MPEG Standard and Stearns. Dependent claim 3 is allowable at least for the same reasons.” *Id.* (citing *In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“Dependent claims are nonobvious under § 103 if the independent claims from which they depend are nonobvious.”)). Based on the record before us, however, we are persuaded that Petitioner provides a sufficiently detailed explanation regarding the teachings of the combination of Bowes, MPEG, and Stearns, and the reasons for combining the teachings of those references to achieve the limitations of claim 3. Pet. 47–49; *see* Ex. 1030 ¶¶ 175–179.

### 3. Conclusion

On this record, Petitioner has demonstrated by a preponderance of the evidence that claim 3 is unpatentable as obvious over the combination of the teachings of Bowes, MPEG, and Stearns.

C. Claim 4 — Obviousness over Bowes, MPEG, and Shanley

Petitioner argues that claim 4 is unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Shanley. Pet. 49–50.

1. Shanley (Ex. 1019)

In Shanley, simultaneously-received bus masters' requests are assigned one of two priority groups. Ex. 1019, 79–81. An arbiter may give greater priority to bus masters in the first group than the second group. *Id.* In particular, “[t]he arbiter can be programmed or designed to treat each group as rotational priority within the group and rotational priority between the two groups. This is pictured in figure 6-2.” *Id.* at 80. “The masters in the first group are permitted to access the bus more frequently than those that reside in the second group.” *Id.* at 81.

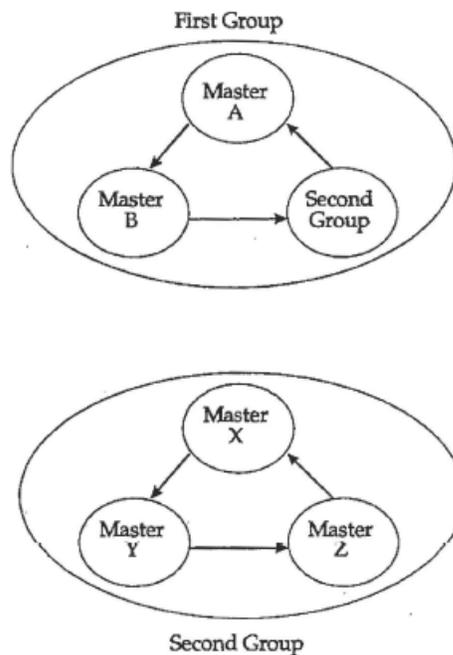


Figure 6-2. Example Arbitration Scheme

Shanley explains that Master A has priority over Master B and Master B has priority over the “Second Group,” i.e., Masters X, Y, and Z. *Id.* at 80–81. Thus, in Shanley’s exemplary arbitration scheme, the arbitration/priority sequence would be “A → B → X → A → B → Y → A → B → Z → A → B → X, and so on.” Pet. 20 (citing Ex. 1019, 80).

## 2. Analysis

Claim 4 depends directly from independent claim 1. As discussed above, we are persuaded that Petitioner has established by a preponderance of the evidence that independent claim 1 would have been obvious over the combination of Bowes and MPEG. *See supra* Section IV.A. Petitioner relies upon Shanley only for the additional limitations recited in dependent claim 4. Pet. 49–50. We are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Shanley teaches or suggests these additional limitations and that a person of ordinary skill in the art would have had reason to combine Shanley’s teachings with those of Bowes and MPEG. *Id.* Moreover, Patent Owner does not dispute that Shanley teaches or suggests the additional limitations of claim 4 or that a person of ordinary skill in the art would have had reason to combine Shanley’s teachings with those of Bowes and MPEG. PO Resp. 42; *see* Ex. 1030 ¶¶ 126–127, 180–181 (arguing persuasively that Shanley shows the additional limitations of claim 4 and that a person of ordinary skill in the art would have had reason to modify the combined teachings of Bowes and MPEG in view of the teachings of Shanley to achieve the challenged claim); *see also* Paper 13, 6 (arguments not raised in the Patent Owner Response are deemed waived).

Instead, Patent Owner contends that Shanley does not teach or suggest the limitations of claim 1 allegedly missing from the combined teachings of

Bowes and MPEG. PO Resp. 42. Patent Owner contends only that “independent claim 1 is also not obvious in view of the proposed combination of Bowes, the MPEG Standard and Shanley. Dependent claim 4 is allowable at least for the same reasons.” *Id.* (citing *Fine*, 837 F.2d at 1076 (discussed above)). Based on the record before us, however, we are persuaded that Petitioner provides a sufficiently detailed explanation regarding the teachings of the combination of Bowes, MPEG, and Shanley, and the reasons for combining the teachings of those references to achieve the limitations of claim 4. Pet. 49–50; *see* Ex. 1030 ¶¶ 126–127, 180–181.

### 3. *Conclusion*

On this record, Petitioner has demonstrated by a preponderance of the evidence that claim 4 is unpatentable as obvious over the combination of the teachings of Bowes, MPEG, and Shanley.

#### D. *Motion for Observations*

Patent Owner filed a Motion for Observations regarding Dr. Stone’s cross-examination. Paper 36 (“Obs.”). Petitioner, in turn, filed a Response. Paper 45 (“Obs. Resp.”). To the extent Patent Owner’s Motion for Observations pertains to testimony purportedly impacting Dr. Stone’s credibility, we have considered Patent Owner’s observations and Petitioner’s responses in rendering this Final Written Decision, and accorded Dr. Stone’s testimony appropriate weight in view of Patent Owner’s observations and Petitioner’s response to those observations. *See* Obs. 1–8; Obs. Resp. 1–4.

## VI. CONCLUSION

For reasons stated above, we conclude that Petitioner has established by a preponderance of the evidence that the combined teachings of Bowes and MPEG, alone or in combination with the teachings of Stearns or

IPR2015-01501  
Patent 7,777,753 B2

Shanley, would have rendered claims 1–4 of the '753 patent obvious to one of ordinary skill in the art at the time of the invention.

#### VII. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–4 of the '753 patent are held unpatentable;

FURTHER ORDERED that Patent Owner's Motion for Observations is taken into consideration; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2015-01501  
Patent 7,777,753 B2

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